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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/615,050	07/07/2003	Sean E. Eilert	42P15837	8003

7590 09/12/2005

Michael A. Bernadicou
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
Seventh Floor
12400 Wilshire Boulevard
Los Angeles, CA 90025

EXAMINER	
NGUYEN, HIEP T	
ART UNIT	**PAPER NUMBER**
2187	

DATE MAILED: 09/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/615,050	EILERT, SEAN E.	
	Examiner	Art Unit	
	Hiep T. Nguyen	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-43* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office action is a response to the communication filed July 7, 2003. Claims 1-43 are presented for examination.

Drawings

2. Figures 1-2 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

    a. A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-43 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art (APA) as described in the background of the invention [specification pages 1-2 and figures 1-2].

    a. <u>As per claims1 and 5-6</u>

        i. The APA teaches an apparatus comprising:

            1. A first addressable device (104) associated with a first device identifier (ID) [spec., page 2, lines 14-15];

2. A second addressable device (106) stacked adjacent the first addressable device, wherein the second addressable device is coupled to the first addressable device [through the substrate 102 and the bond wires 116; see the spec., page 2, lines 7-9].

ii. The APA, however, does not teaches that the second memory device includes a circuit to generate a second device ID as a function of the first device ID.

iii. In stack memories, it has been known and widely practiced in the pertinent art that adjacent memory location or entry always has an address or identification that is linearly related to the current location or entry. Furthermore, it has also been known and commonly practiced in the pertinent art that generating an address or a pointer value associated with a next memory location or entry by adding or subtracting the current memory address or pointer value by a constant.

iv. One having ordinary skill in the art, who is familiar with such stack pointer/address/identification generating feature, looks at the teaching of the prior art, would leads he or she to further employ the commonly used logic for generating a second memory device ID by adding or subtracting the current ID [i.e., the first device ID]. It would have been obvious because memory units in a stacked memory device are identified in the same manner as stacked entries in a stack memory. Furthermore, adder logic is simple to construct.

v. Accordingly, it would have been obvious to one having ordinary skill in the pertinent art to further employ a logic such as an adder circuit into the APA second addressable device for generating a second ID by adding the ID of the first addressable dive with a constant. The simplicity of an adder circuit provide sufficient suggestion and motivation to one having ordinary skill in the pertinent art to do such logic adding in the APA second addressable device.

b. As per claims 2-3: flash memory, DRAM, SRAM, etc, have also been known and commonly used as memory devices in stacked memories.

c. As per claim 4: the APA directly teaches the further claimed limitation of "wherein the first device is encoded [spec., p2, ll.5-6]

d. As per claims 7-10: the claimed apparatus basically encompasses the same elements as that of claims 1-6. Accordingly, claims 7-10 are also rejected for the same reason as set forth for that of claims 1-6.

e. As per claim 11, the claimed apparatus basically encompasses the same scope as that of claim 1 with an exception of the newly added limitation of "a through-silicon via". Using a through-silicon via in a memory device to connect two or more memory elements has also been known and commonly used in the pertinent art. Accordingly, it would also been obvious to one having ordinary skill in the art to use a through-silicon via to connect two or more memory elements in the APA stacked memory device.

f. As per claims 12-15, 20-22and 25: the claimed method basically comprises the steps that are carried out by the corresponding elements in claims 1-6. Accordingly claims 12-15 are also rejected for the same reasons as set forth for claims 1-6.

g. As per claim 17: the claimed method basically comprises the steps that are carried out by the corresponding elements in claim 11. Accordingly claim 17 is also rejected for the same reason as set forth for claim 11.

h. As per claims 18-19: optically or capacitively coupling one memory element to another has also been known and commonly practiced in the pertinent art. Accordingly it would have been obvious to one having ordinary skill in the art at the time the invention was made to capacitively or optically couple the APA first memory device to the second memory device.

i. As per claims 23-24: using an active or a passive logical shifter in the place of an adder circuit has also been known and commonly used in the art. Accordingly, it would also as been obvious to one having ordinary skill in art to use an active or passive logical shifter to generate a second device ID.

j. As per claims 26-37: the claimed method basically encompass the same scope as that of claims 12-25. Accordingly, claims 26-37 are also rejected for the same reason as set forth for claims 12-25.

k. As per claims 38-43: the claimed system basically encompasses the stacked memory device as that in claims 1-6 and further comprises a processor that is coupled to an RF interface. Stacked memory such as that of the APA has been known and widely used in application that has a processor coupled to an RF interface [e.g., cellular phones, palm computing devices, etc.]. Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to utilized the stacked memory device in a system that has processor coupled to an RF interface.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.
   a. Aidan et al., 6,654,871, teaches an adder/subtractor for generating an updated pointer by adding a constant to a current stack pointer.
   b. Kudo et al., 6,560,692, teaches a logic for adding a current stack pointer to a selected offset value to generate a new stack pointer.
   c. Bhattacharyya, US 2004/0155298, teaches a stacked memory device using SRAM memory arrays.
   d. Martines et al., 2002/0131303, teaches a stacked memory device that uses the combination of flash non-volatile memories and faster SRAM memories.
6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hiep T. Nguyen whose telephone number is (571) 272-4197. The examiner can normally be reached on Monday-Friday from 9:30 am to 6:00 pm.
7. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

8. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hiep T Nguyen
Primary Examiner
Art Unit 2187

HTN